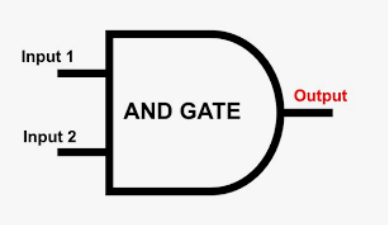
Logic Gates 1.0.0

AND Gate

An AND gate is a logic gate having two or more inputs and a single output. An AND gate operates on logical multiplication rules. In this gate, if either of the inputs is low (0), then the output is also low. If all of the inputs are high (1), then the output will also be high. An AND gate can have any number of inputs, although 2 input and 3 input AND gates are the most common.

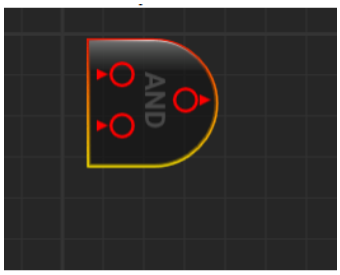
There are two binary digits – 0 and 1. We just told that an AND gate performs a binary multiplication of binary digits. In multiplying 0 with 0 we will get 0, 1 with 0 or 0 with 1 we will get 0. Only we get 1 when 1 is multiplied by 1.

Symbol For AND Gate:

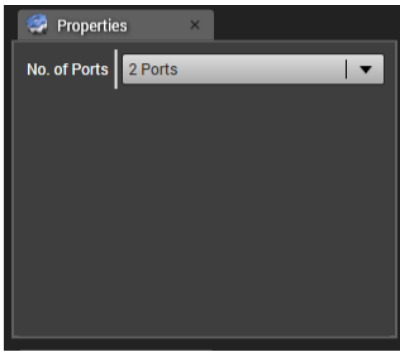


Case 1: Default Settings

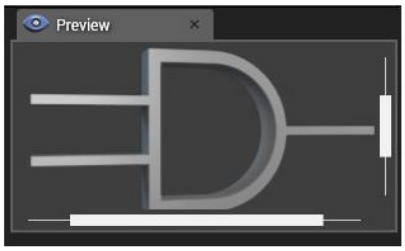
1. Default Node Style



2. Default Property Window

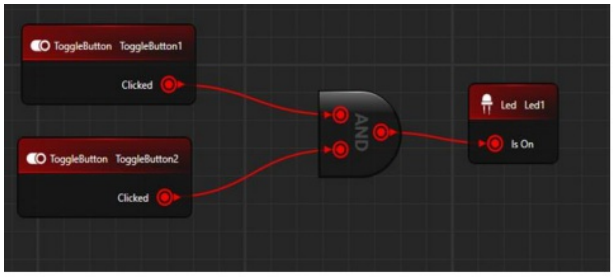


3. Default Preview

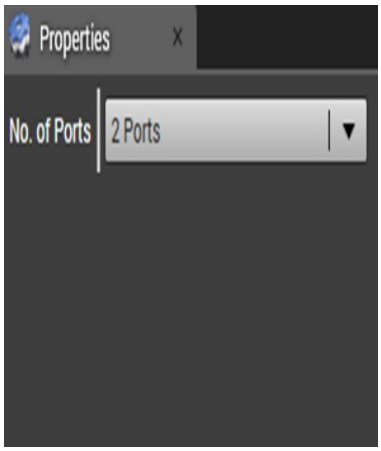


Case 1: Testing for Two Ports

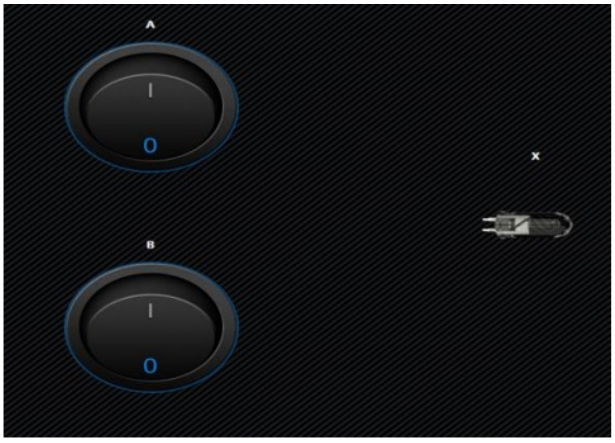
1. Node Style



2. Property Window



View in HOST



Expected Result With Two Ports or PINS(Truth Table for Two ports)

Statement:- A HIGH output (1) results only if all the inputs to the AND gate are HIGH (1). If none or not all inputs to the AND gate are HIGH, LOW output results.

Note:-Similarly, it can be tested for other ports.

NAND Gate

In digital electronics, a NAND gate (NOT-AND) is a logic gate which produces an output which is false only if all its inputs are true; thus its output is complement to that of an AND gate. A LOW (0) output results only if all the inputs to the gate are HIGH (1); if any input is LOW (0), a HIGH (1) output results.

If the truth table for a NAND gate is examined or by applying De Morgan's Laws, it can be seen that if any of the inputs are 0, then the output will be 1. To be an OR gate, however, the output must be 1 if any input is 1. Therefore, if the inputs are inverted, any high input will trigger a high output.

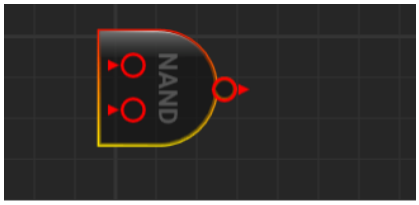
Q = **A** NAND **B**

Truth Table

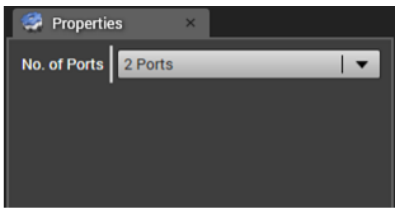
Input A	Input B	Output Q
0	0	1
0	1	1
1	0	1
1	1	0

Case 1: Default Settings

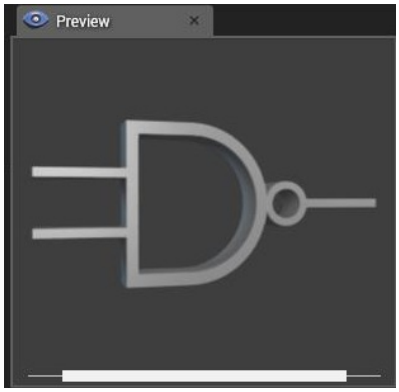
1. Default Node Style



2. Property Window

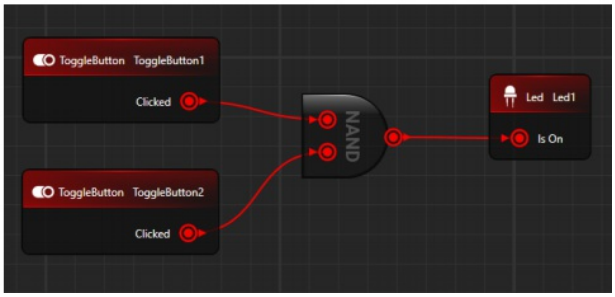


3. Default Preview

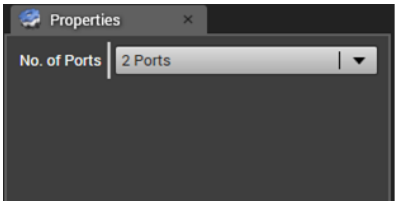


Case 1: Testing for Two Ports

1. Node Style



2. Property Window



3. View in HOST

Note:-Similarly, it can be tested for other ports

NOR Gate

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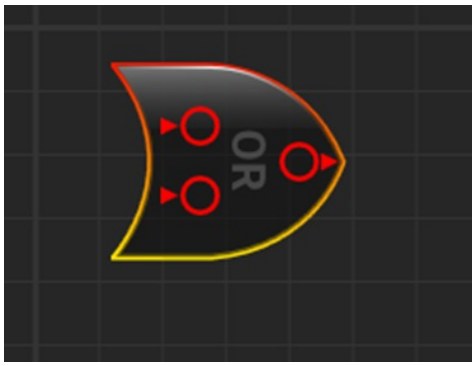
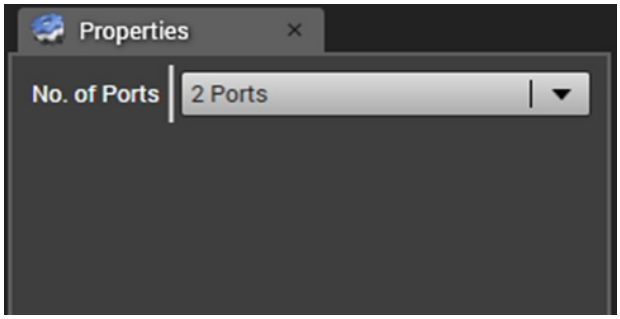
OR Gate

Case 1: Default Settings

(A) Default Node Style



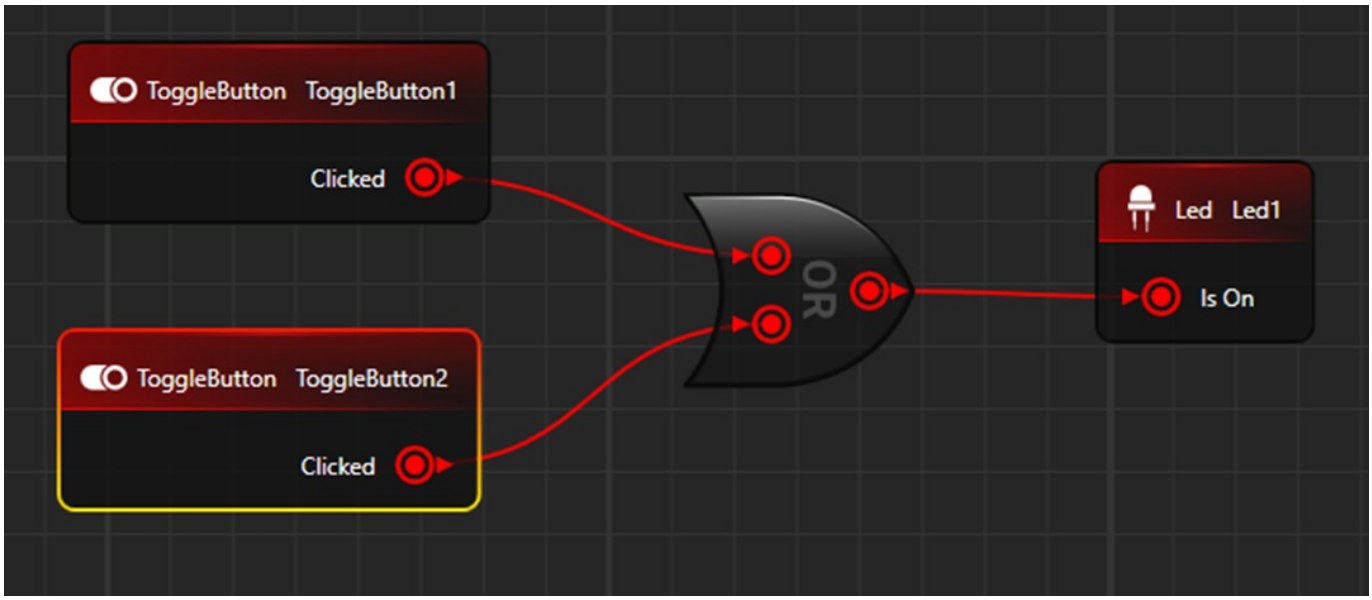
(B) Default Property Window



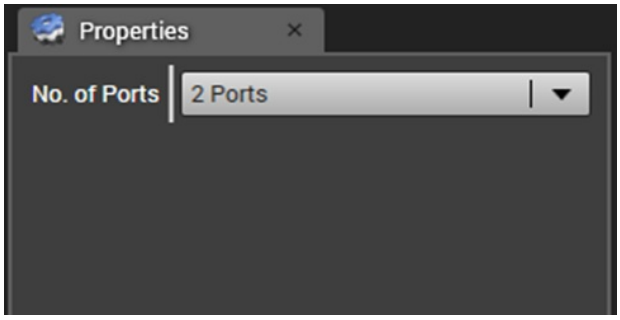
(C) Default Preview

Case 1: Testing for Two Ports

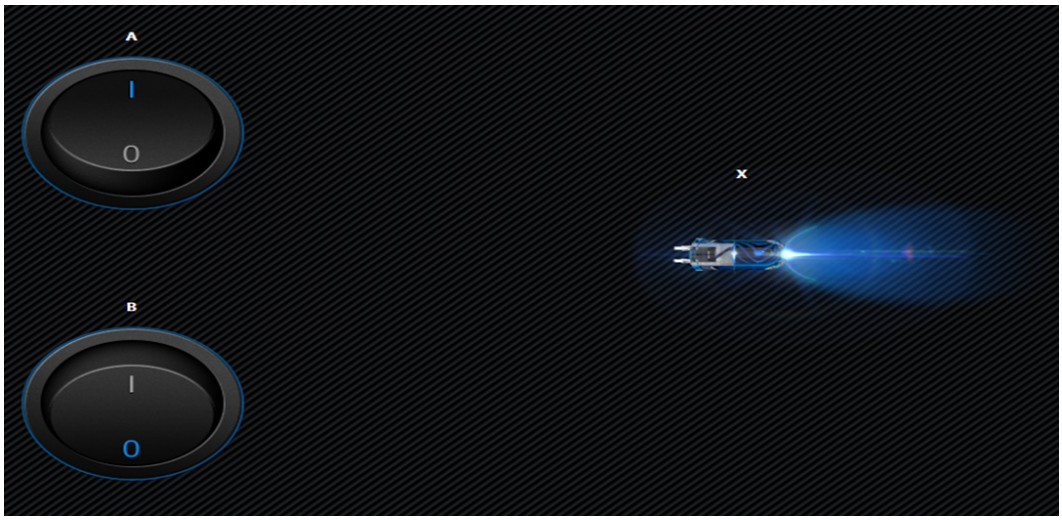
(A) Node Style



(B) Property Window



(C) View in HOST



Statement:- A HIGH output (1) results if one or both the inputs to the gate are HIGH (1). If neither input is high, a LOW output (0) results.

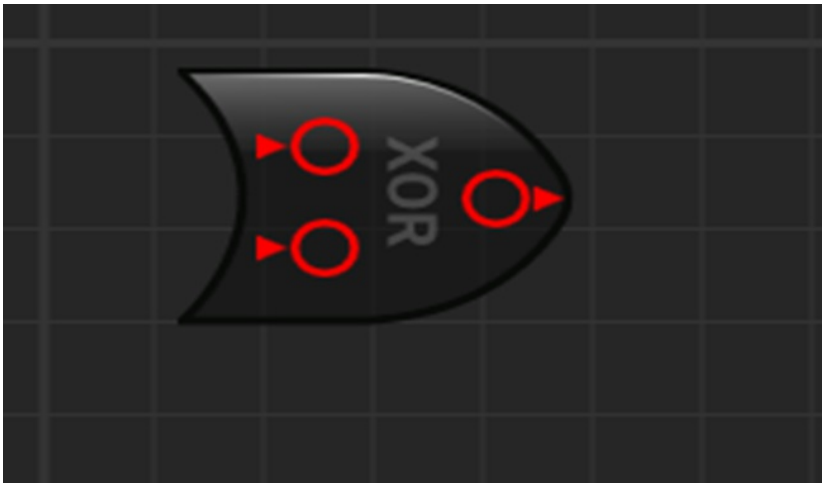
INPUT		OUTPUT
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

Note:-Similarly, it can be tested for other ports.

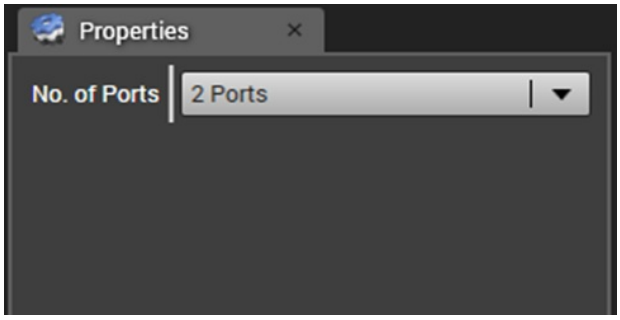
XOR Gate

Case 1: Default Settings

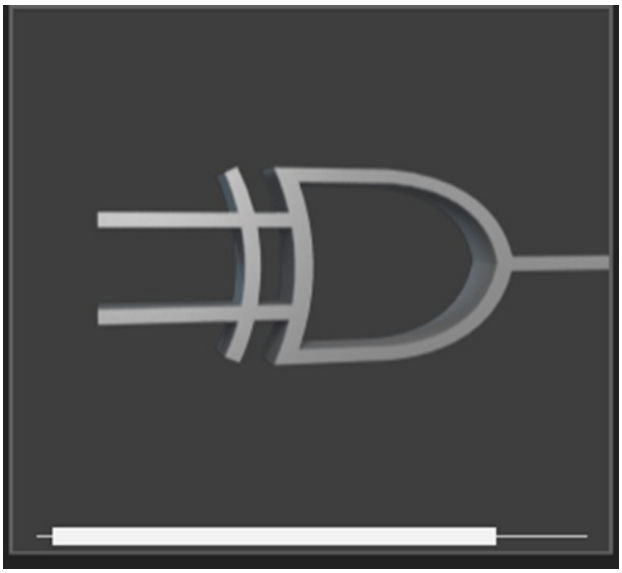
(A) Default Node Style



(B) Default Property window

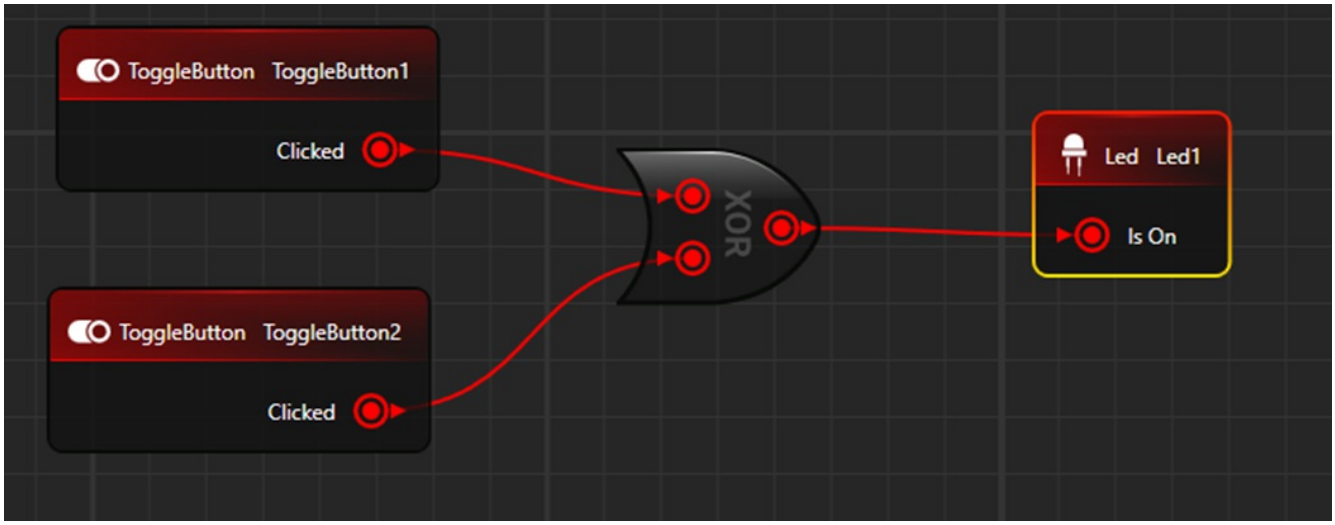


(C) Default Preview Window

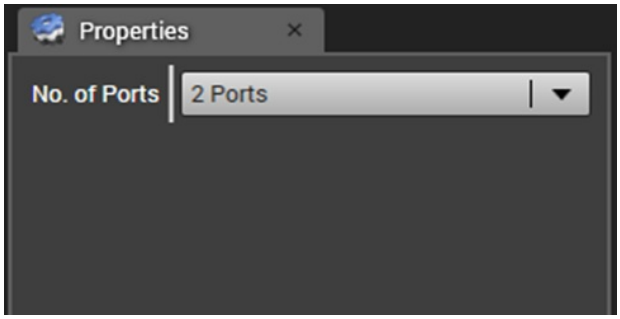


Case 1: Testing for Two Ports

(A) Node Style



(B) Property window



(C) View in HOST

Statement: A true (1 or HIGH) output when the number of true inputs is odd.

INPUT		OUTPUT
A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

Three Ports

Inputs			Output
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Four Ports

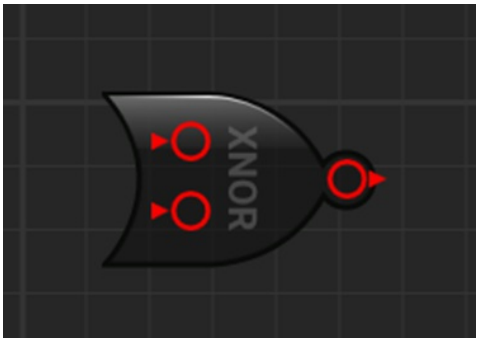
Input A	Input B	Input C	Input D	Output Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Note:-Similarly, it can be tested for other ports.

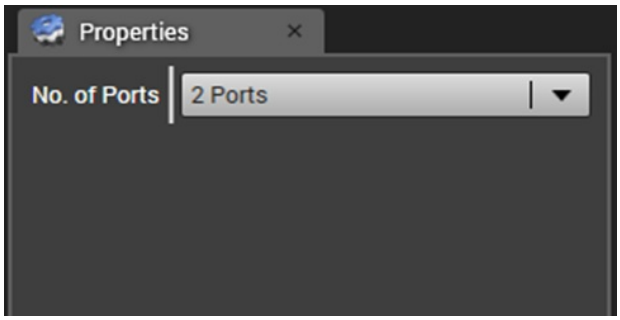
XNOR

Case 1: Default Settings

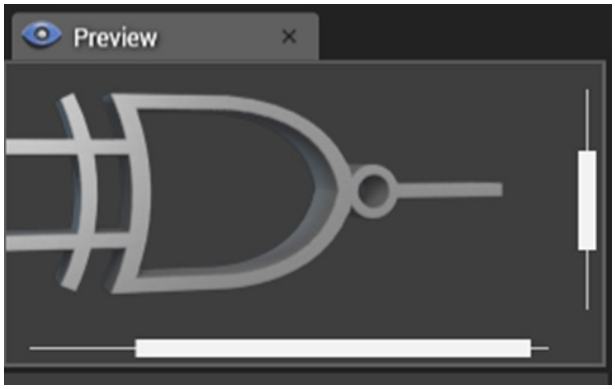
(A) Default Node Style



(B) Default Property window

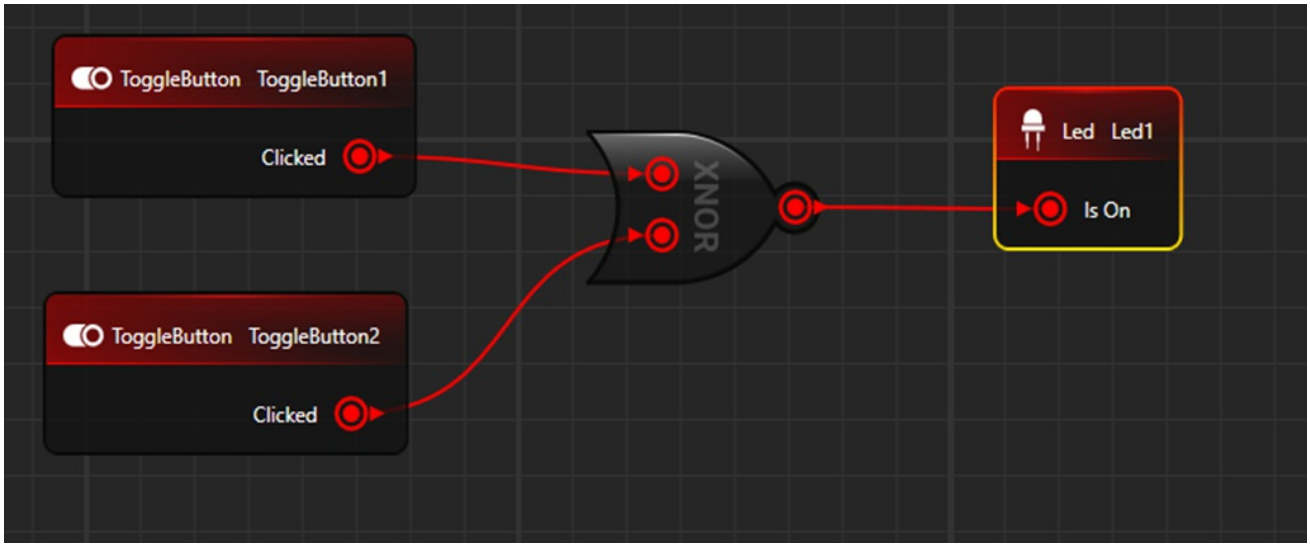


(C) Default Preview Window

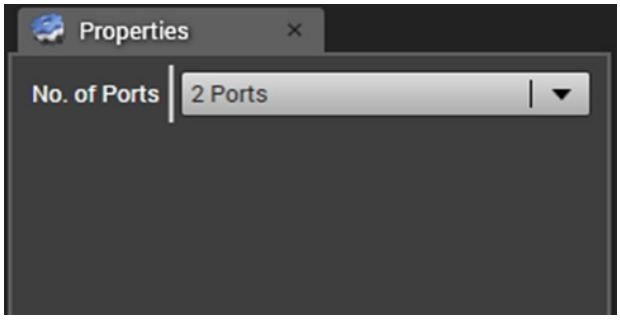


Case 1: Testing for Two Ports

(A) Node Style



(B) Property window



(C) View in HOST

Statement: A high output (1) results if both of the inputs to the gate are the same. If one but not both inputs are high (1), a low output (0) results.

Input		Output
A	B	A XNOR B
0	0	1
0	1	0
1	0	0
1	1	1

Three Ports

Inputs			Output
A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

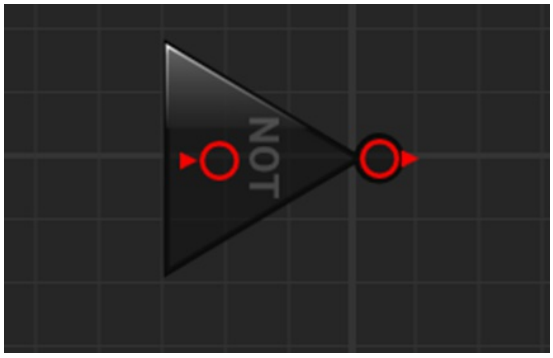
Four Ports

Input A	Input B	Input C	Input D	Output Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

NOT Gate

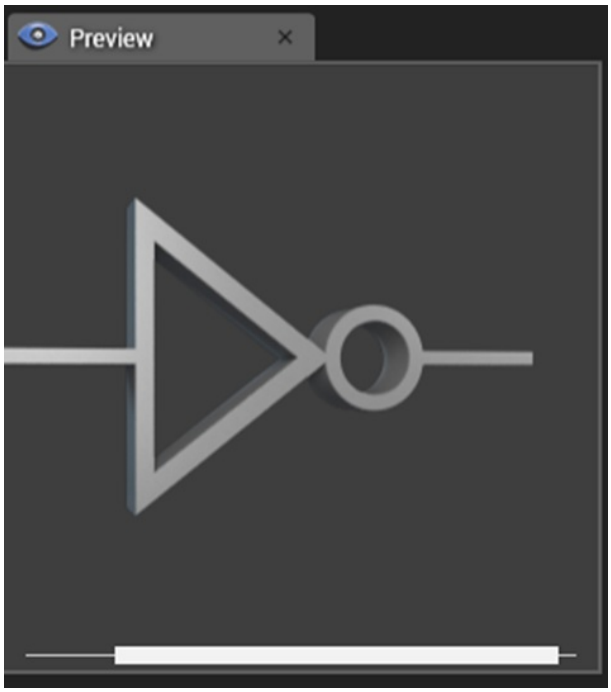
Case 1: Default Settings

(A) Default Node Style



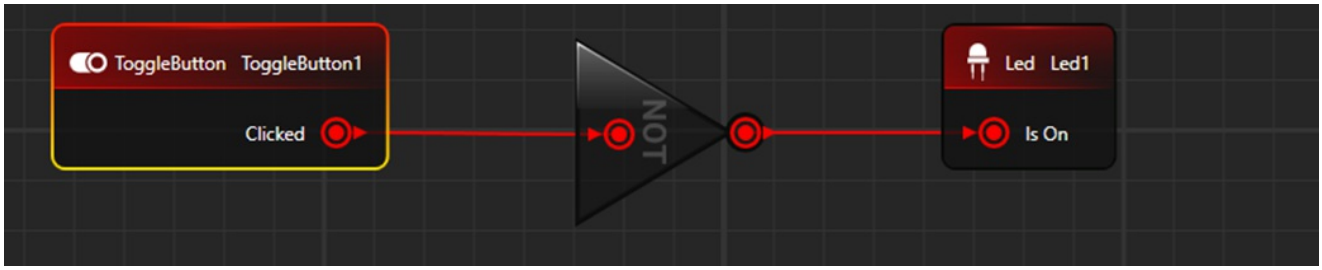
(B) Default Property Window

(C) Default Preview Window



Case 1: Testing for one Port/Pin

(A) Node Style



(B) View in HOST

Statement: An inverter or NOT gate is a logic gate which implements logical negation.

INPUT	OUTPUT
A	NOT A
0	1
1	0

Note:-It will have only single input port.